

# **Method of Processing Signed Loads with the Same Latency as Unsigned Loads in a High-Frequency Processor**

## **ABSTRACT**

A method for reducing signed load latency in a microprocessor has been developed. The method includes transferring a part of data to an aligner via a bypass, and generating a sign bit from the part of the data. The sign bit is transferred to the aligner along the bypass, and the data is separately transferred to the aligner along a data path.

16169\_2.DOC

16169\_2.DOC